"CO DIALTONE LEARNING SEQUENCE" FLOW MODEL

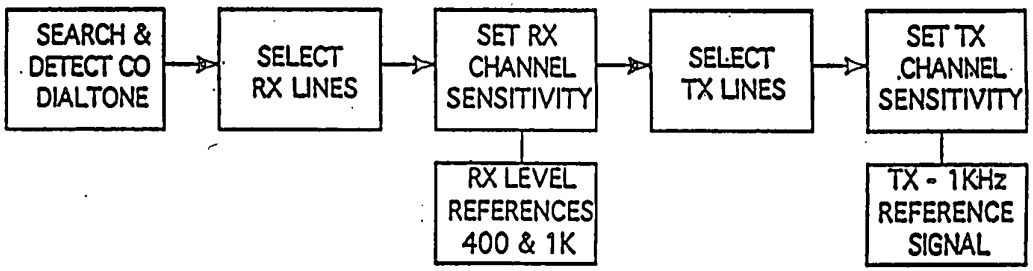


FIG. 1

"AUTOMATED 800 LEARNING SEQUENCE" FLOW MODEL

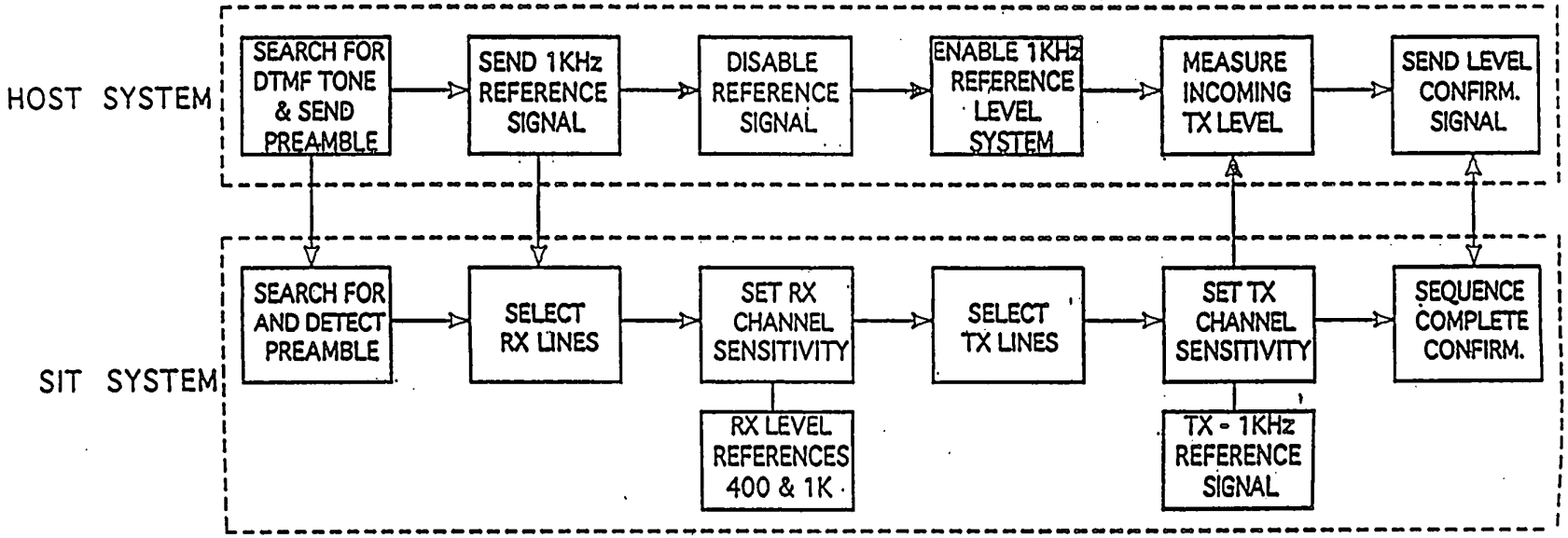
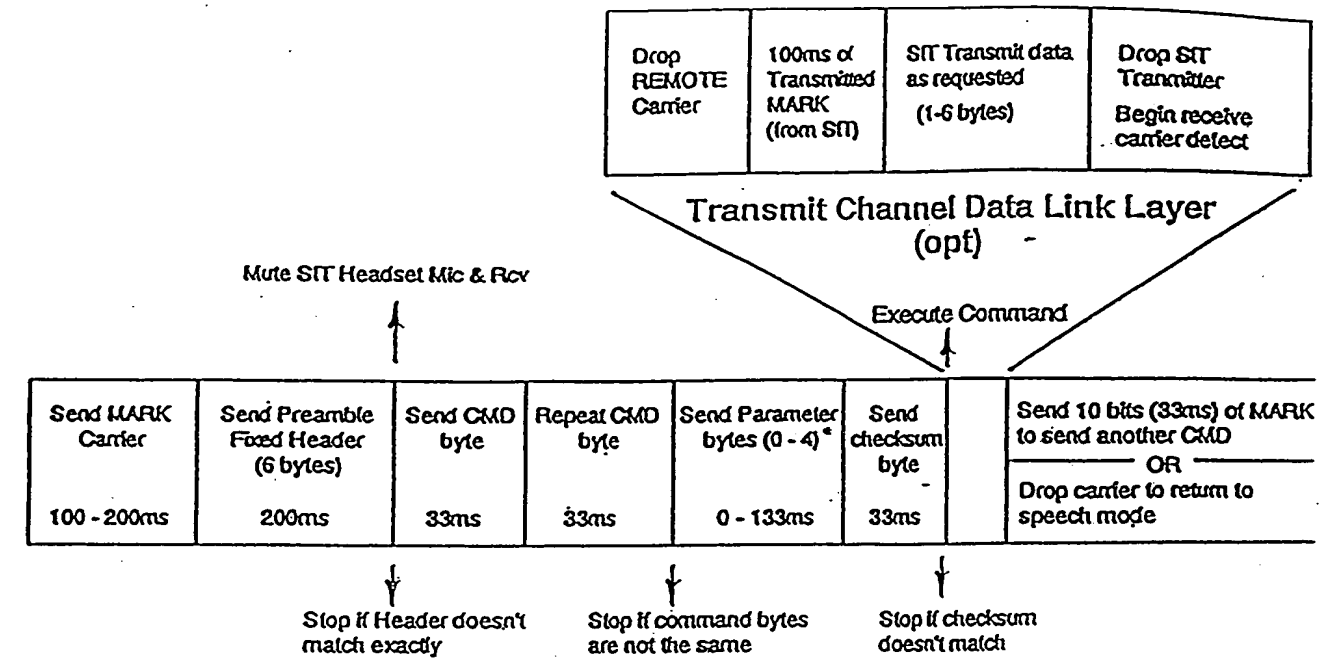


FIG. 2



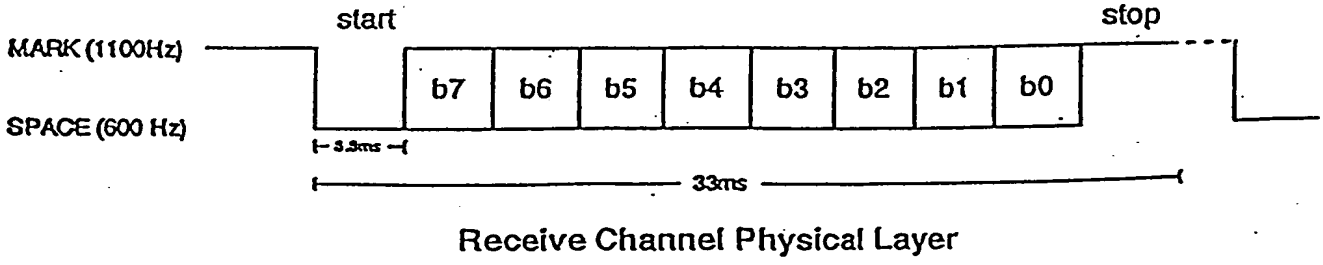
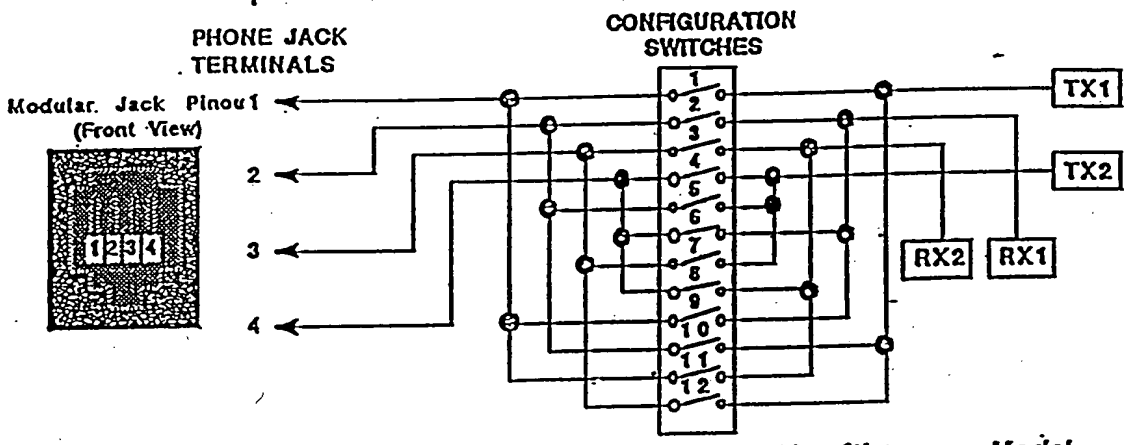


FIG. 3

0202050-050505

Smart Interface Technology (SIT) Project
Preliminary Line Configuration Switching Algorithms and Model

Equivalent Line Configuration Switching Model



Dialtone Detection	Rx Pinout	Tx Pinout Sequence	Algorithm Ref. No.	Model Sw. "ON"
Pins 2 & 3	Pins 2 & 3	Pins 1 & 4 (Primary)	1	1,2,3,4
Pins 2 & 3	Pins 2 & 3	Pins 1 & 2 (2nd Try)	2	1,2,3,5
Pins 2 & 3	Pins 2 & 3	Pins 1 & 3 (3rd Try)	3	1,2,3,7
Pins 2 & 3	Pins 2 & 3	Pins 4 & 2 (4th Try)	4	2,3,4,10
Pins 2 & 3	Pins 2 & 3	Pins 4 & 3 (5th Try)	5	2,3,4,12
Pins 2 & 4	Pins 2 & 4	Pins 1 & 3 (Primary)	6	1,2,7,8
Pins 2 & 4	Pins 2 & 4	Pins 1 & 2 (2nd Try)	7	1,2,5,8
Pins 2 & 4	Pins 2 & 4	Pins 1 & 4 (3rd Try)	8	1,2,4,8
Pins 2 & 4	Pins 2 & 4	Pins 3 & 2 (4th Try)	9	2,5,8,12
Pins 2 & 4	Pins 2 & 4	Pins 3 & 4 (5th Try)	10	2,4,8,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 4 (Primary)	11	2,4,11,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 1 (2nd Try)	12	1,2,11,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 2 (3rd Try)	13	2,5,11,12
Pins 1 & 2	Pins 1 & 2	Pins 4 & 1 (4th Try)	14	1,2,4,11
Pins 1 & 2	Pins 1 & 2	Pins 4 & 2 (5th Try)	15	2,4,10,11
Pins 1 & 3	Pins 1 & 3	Pins 2 & 4 (Primary)	16	3,4,9,11
Pins 1 & 3	Pins 1 & 3	Pins 2 & 1 (2nd Try)	17	1,3,5,9
Pins 1 & 3	Pins 1 & 3	Pins 2 & 3 (3rd Try)	18	3,5,9,12
Pins 1 & 3	Pins 1 & 3	Pins 4 & 1 (4th Try)	19	1,3,4,9
Pins 1 & 3	Pins 1 & 3	Pins 4 & 3 (5th Try)	20	3,4,9,12

FIG. 4

5,550,894 - 08/27/96

Dialtone Detection	Rx Pinout	Tx Pinout Sequence	Algorithm Ref. No.	Model Sw. "ON"
Pins 1 & 4	Pins 1 & 4	Pins 2 & 3 (Primary)	21	7,8,9,10
Pins 1 & 4	Pins 1 & 4	Pins 2 & 1 (2nd Try)	22	1,5,8,9
Pins 1 & 4	Pins 1 & 4	Pins 2 & 4 (3rd Try)	23	4,8,9,10
Pins 1 & 4	Pins 1 & 4	Pins 3 & 1 (4th Try)	24	1,7,8,9
Pins 1 & 4	Pins 1 & 4	Pins 3 & 4 (5th Try)	25	4,8,9,12
Pins 3 & 4	Pins 3 & 4	Pins 1 & 2 (Primary)	26	1,3,5,6
Pins 3 & 4	Pins 3 & 4	Pins 1 & 3 (2nd Try)	27	1,3,6,7
Pins 3 & 4	Pins 3 & 4	Pins 1 & 4 (3rd Try)	28	1,3,4,6
Pins 3 & 4	Pins 3 & 4	Pins 2 & 3 (4th Try)	29	3,6,7,10
Pins 3 & 4	Pins 3 & 4	Pins 2 & 4 (5th Try)	30	3,4,6,10

ALGORITHM REF. NUMBER	SWITCHING MODEL ACTION	ALGORITHM REF. NUMBER	SWITCHING MODEL ACTION
31	Switch 1: "ON"	43	Switch 7: "ON"
32	Switch 1: "OFF"	44	Switch 7: "OFF"
33	Switch 2: "ON"	45	Switch 8: "ON"
34	Switch 2: "OFF"	46	Switch 8: "OFF"
35	Switch 3: "ON"	47	Switch 9: "ON"
36	Switch 3: "OFF"	48	Switch 9: "OFF"
37	Switch 4: "ON"	49	Switch 10: "ON"
38	Switch 4: "OFF"	50	Switch 10: "OFF"
39	Switch 5: "ON"	51	Switch 11: "ON"
40	Switch 5: "OFF"	52	Switch 11: "OFF"
41	Switch 6: "ON"	53	Switch 12: "ON"
42	Switch 6: "OFF"	54	Switch 12: "OFF"

NOTES:

1) Algorithm No. 1 will be the default setting for system power-up, hard or soft resets and "learning" timeout conditions.
2) Ideally all 12 equivalent switches can be selected and switched "on" or "off" independant of the above algorithm's.

FIG. 5

5,995,594 - Dec. 30, 1999

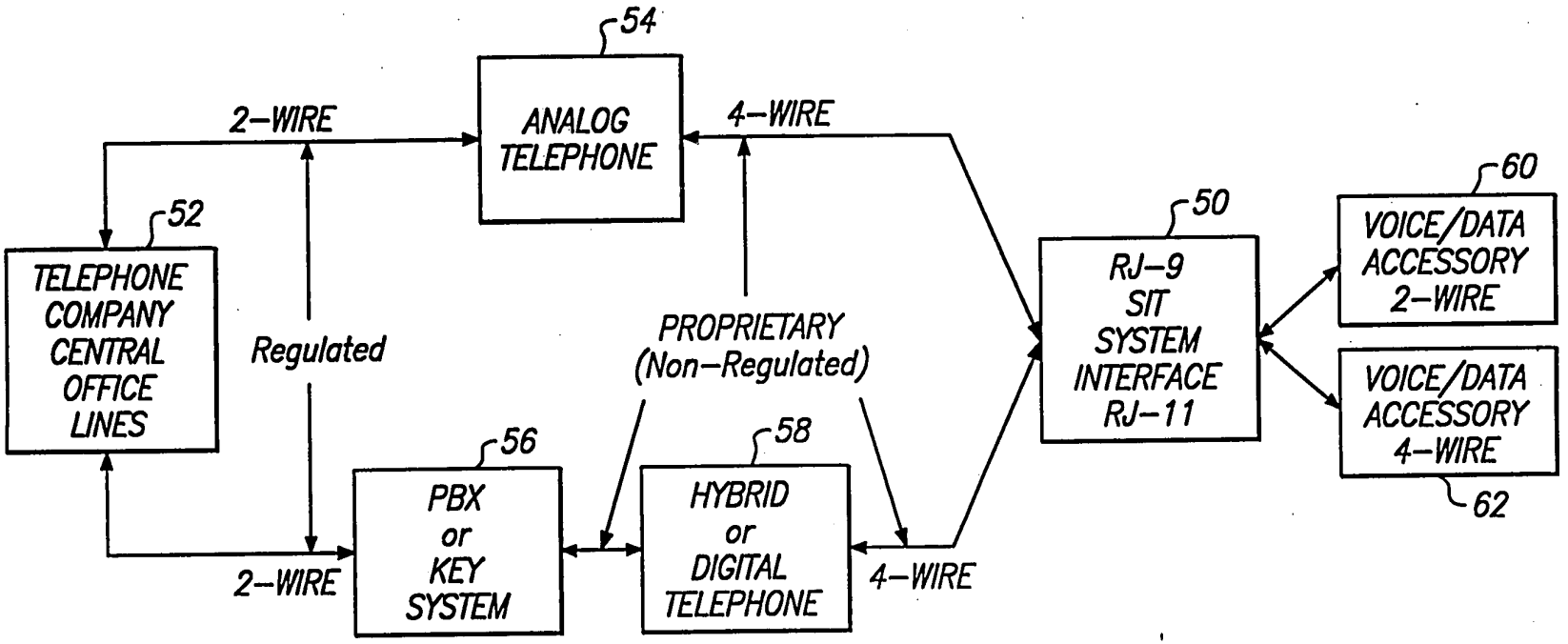

54
ANALOG TELEPHONE
2–WIRE
4–WIRE
52
TELEPHONE COMPANY CENTRAL OFFICE LINES
Regulated
PROPRIETARY (Non–Regulated)
50
RJ–9 SIT SYSTEM INTERFACE RJ–11
60
VOICE/DATA ACCESSORY 2–WIRE
VOICE/DATA ACCESSORY 4–WIRE
62
56
PBX or KEY SYSTEM
58
HYBRID or DIGITAL TELEPHONE
2–WIRE
4–WIRE

FIG. 6

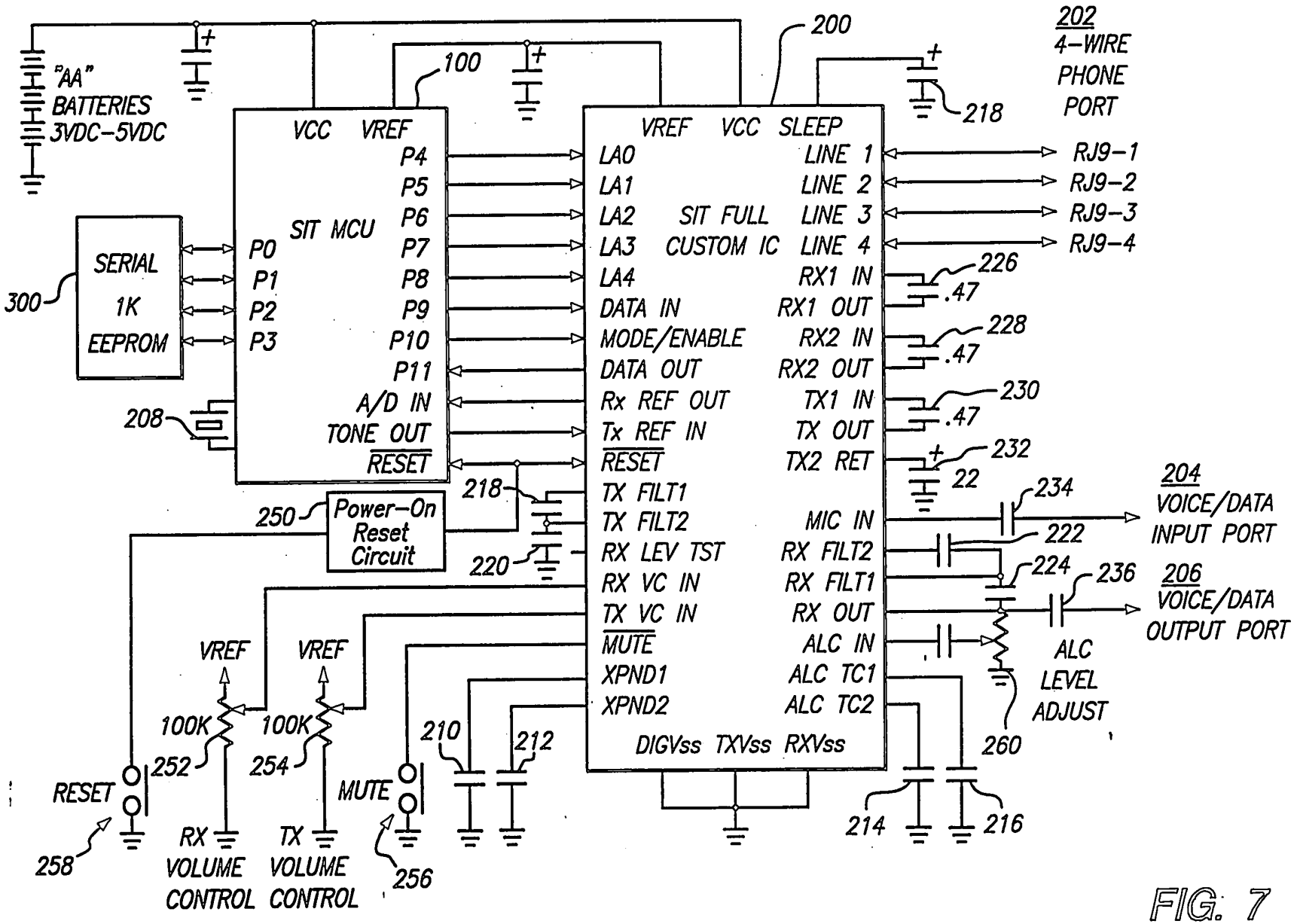

"AA" BATTERIES 3VDC–5VDC
100
200
202 4–WIRE PHONE PORT
218
VCC VREF
P4
P5
P6
P7
P8
P9
P10
P11
A/D IN
TONE OUT
RESET
SIT MCU
P0
P1
P2
P3
SERIAL 1K EEPROM
300
208
VREF VCC SLEEP
LA0
LA1
LA2
LA3
LA4
DATA IN
MODE/ENABLE
DATA OUT
Rx REF OUT
Tx REF IN
RESET
TX FILT1
TX FILT2
RX LEV TST
RX VC IN
TX VC IN
MUTE
XPND1
XPND2
SIT FULL CUSTOM IC
DIGVss TXVss RXVss
LINE 1
LINE 2
LINE 3
LINE 4
RX1 IN
RX1 OUT
RX2 IN
RX2 OUT
TX1 IN
TX OUT
TX2 RET
MIC IN
RX FILT2
RX FILT1
RX OUT
ALC IN
ALC TC1
ALC TC2
RJ9–1
RJ9–2
RJ9–3
RJ9–4
226 .47
228 .47
230 .47
232 22
234
222
224
236
204 VOICE/DATA INPUT PORT
206 VOICE/DATA OUTPUT PORT
ALC LEVEL ADJUST
260
250
Power–On Reset Circuit
218
220
VREF
VREF
100K
100K
252
254
RESET
MUTE
258
256
RX VOLUME CONTROL
TX VOLUME CONTROL
210
212
214
216

FIG. 7

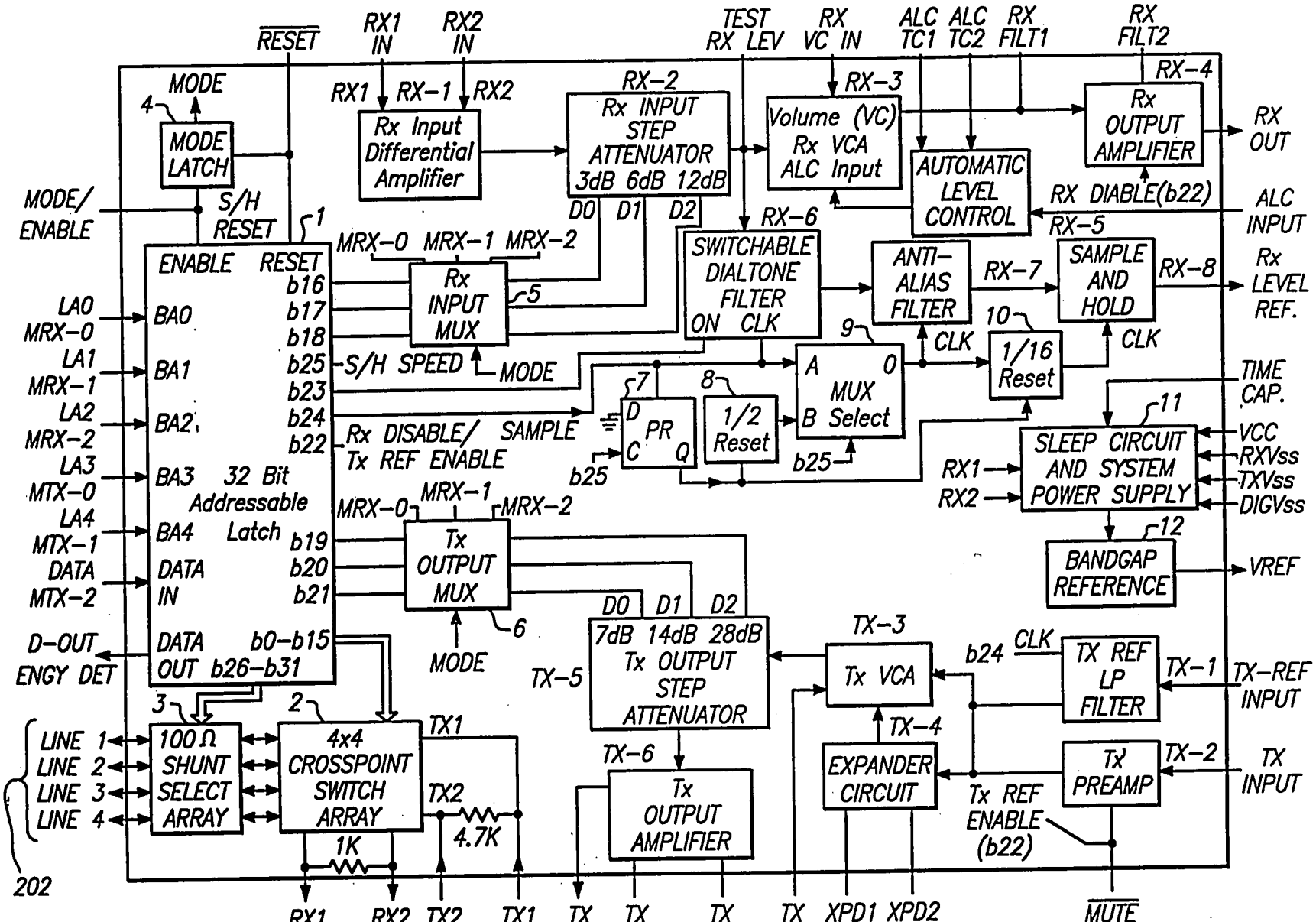

RESET
RX1 IN
RX2 IN
TEST RX LEV
RX VC IN
ALC TC1
ALC TC2
RX FILT1
RX FILT2
MODE
MODE LATCH
RX1
RX-1
RX2
Rx Input Differential Amplifier
RX-2
Rx INPUT STEP ATTENUATOR 3dB 6dB 12dB
RX-3
Volume (VC) Rx VCA ALC Input
RX-4
Rx OUTPUT AMPLIFIER
RX OUT
AUTOMATIC LEVEL CONTROL
RX DIABLE(b22)
RX-5
ALC INPUT
MODE/ ENABLE
S/H RESET
D0 D1 D2
RX-6
SWITCHABLE DIALTONE FILTER ON CLK
ANTI-ALIAS FILTER
RX-7
SAMPLE AND HOLD
RX-8
Rx LEVEL REF.
MRX-0 MRX-1 MRX-2
Rx INPUT MUX
ENABLE RESET
b16 b17 b18 b25 b23 b24 b22
LA0 MRX-0
LA1 MRX-1
LA2 MRX-2
LA3 MTX-0
LA4 MTX-1
DATA MTX-2
BA0 BA1 BA2 BA3 BA4 DATA IN
32 Bit Addressable Latch
DATA OUT b26-b31
D-OUT ENGY DET
S/H SPEED
MODE
Rx DISABLE/ SAMPLE
Tx REF ENABLE
b25
D PR C Q
1/2 Reset
A MUX B Select
CLK
1/16 Reset
TIME CAP.
SLEEP CIRCUIT AND SYSTEM POWER SUPPLY
VCC
RXVss
TXVss
DIGVss
RX1
RX2
BANDGAP REFERENCE
VREF
Tx OUTPUT MUX
7dB 14dB 28dB Tx OUTPUT STEP ATTENUATOR
TX-5
Tx VCA
TX-3
b24 CLK
TX REF LP FILTER
TX-1
TX-REF INPUT
TX-4
EXPANDER CIRCUIT
Tx PREAMP
TX-2
TX INPUT
Tx REF ENABLE (b22)
LINE 1
LINE 2
LINE 3
LINE 4
100 Ω SHUNT SELECT ARRAY
4x4 CROSSPOINT SWITCH ARRAY
TX1
TX2
4.7K
1K
TX-6
Tx OUTPUT AMPLIFIER
202
RX1 OUT
RX2 OUT
TX2 RTN
TX1 IN
TX OUT
TX FILT1
TX FILT2
TX VCIN
XPD1 CAP
XPD2 CAP
MUTE

FIG. 8

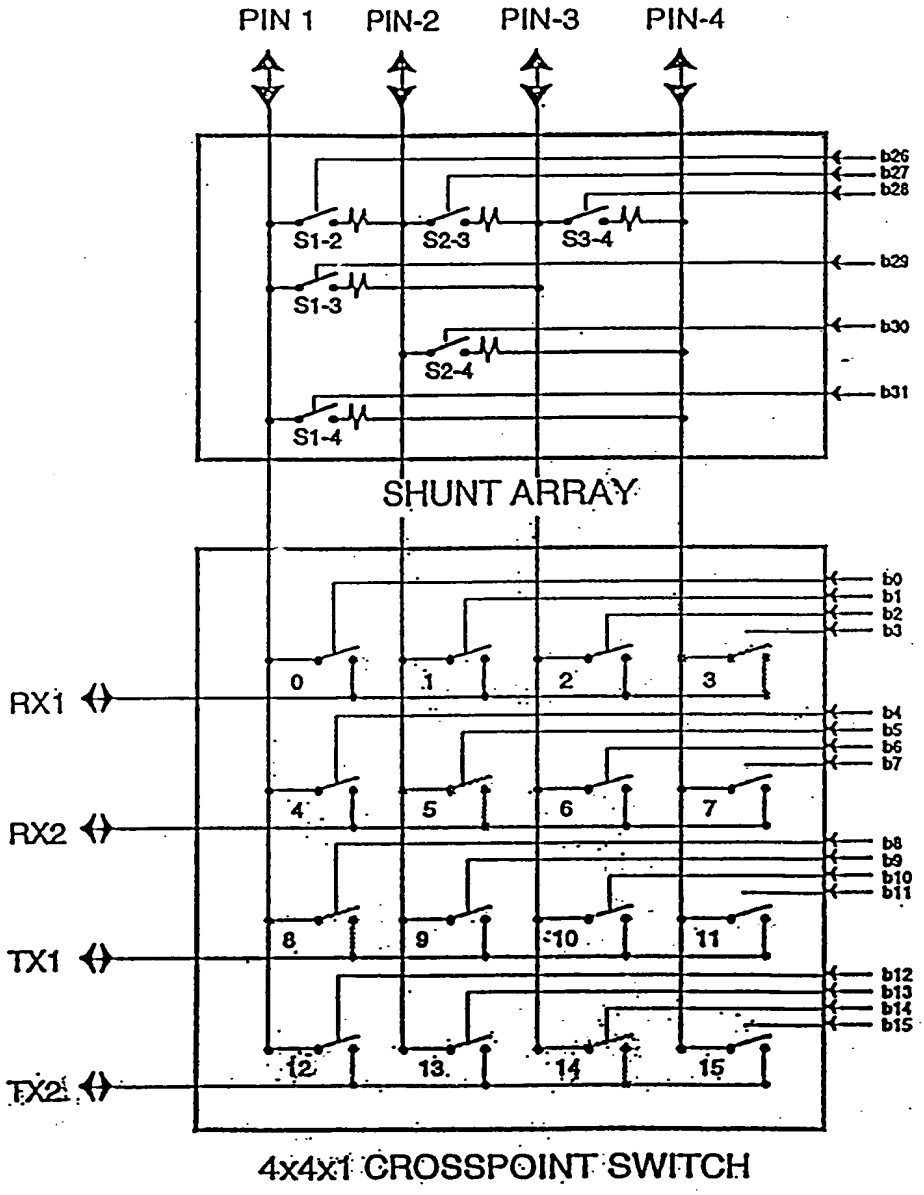

PIN 1
PIN-2
PIN-3
PIN-4
S1-2
S2-3
S3-4
S1-3
S2-4
S1-4
b26
b27
b28
b29
b30
b31
SHUNT ARRAY
b0
b1
b2
b3
b4
b5
b6
b7
b8
b9
b10
b11
b12
b13
b14
b15
RX1
RX2
TX1
TX2
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
4x4x1 CROSSPOINT SWITCH

FIG. 9